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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/941,079	08/28/2001	Kun-Yung K. Chang	R1-P101	5752
38456	7590	12/23/2005	EXAMINER	
DENIRO/RAMBUS			CHANG, EDITH M	
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SAN FRANCISCO, CA 94105			PAPER NUMBER	
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DATE MAILED: 12/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/941,079

Applicant(s)

CHANG ET AL.

Examiner

Edith M. Chang

Art Unit

2637

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 13 October 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-43, 45 and 47-59 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 19-34, 45, 47-51 and 59 is/are allowed.
- 6) ☒ Claim(s) 1-18, 35, 36, 38, 40-43 and 52-58 is/are rejected.
- 7) ☒ Claim(s) 37 and 39 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Response to Arguments/Remarks

1. Applicant's arguments filed on October 13, 2005 have been fully considered but they are not persuasive.

Regarding claims 1, 11 and 52

Argument: Applicants argue that the select circuit of Kyles et al. does not output "one of the" the FASTER signal and the SLOWER signal "as the selected control signal," but rather the select circuit outputs a $TUNE_0$ - $TUNE_{N-1}$ signal which is the value of shift register 730.

Response: In FIG.5 Kyles et al. ('680) discloses MUXes 516 & 518, charge pump 530 and filter 540 (as a selected circuit) to output the TUNE, wherein the charge pump 530 charges filter 540 responsive to the UP signal, which correspondingly increases VTUNE, and discharges filter 540 responsive to the DOWN signal, which correspondingly decreases VTUNE. The output voltage VTUNE of filter 540 is the TUNE signal (column 6, lines 45-50 '680), and the UP signal is SLOWER selected by the SELECT, the DOWN signal is FASTER selected by the SELECT when the 310 delayed, and vice versa (column 6, lines 20-30), hence, the TUNE of the output of the selected circuit (the last stage of the selected circuit, filter 540) is responsive to the SELECT to select from one of the SLOWER signal and the FASTER signal, to decrease or to increase the output of the selected circuit VTUNE, to be output as a selected control signal TUNE.

In FIG.7, the charge pump 530 and filter 540 (of FIG.5) are replaced with a shift register 730 that the selected circuit (MUXes 526 & 518 and the shift register 730) output the TUNE being responsive to the one of the LEFT signal and the RIGHTS signal in turns one of the SLOWER and the FASTER.

Therefore, Kyles et al. discloses a selected circuit both in FIG.5 and FIG.7 being responsive to a select signal (SELECT) to select form one of the first control signal (SLOWER) and the second control signal (FASTER) to be output as a selected control signal to a phase adjust circuit as recited in the claims.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-18, 35-36, 38, and 40-43 are rejected under 35 U.S.C. 102(b) as being anticipated by Kyles et al. (US 6,008,680).

Regarding claims 1 & 11, in Fig.7, Kyles et al. teaches a circuit of receiving clocking signal and its method, the circuit comprises a phase detect 520 (as the control circuit) receiving a RECEWE DATA (as an input signal) to generate a SLOWER (as the first control signal) based on the phase difference of the RECEWE DATA and the

RECOVERED CLOCK (column 6 lines 23-32); the MUX 516, the MUX 518 and the shift register 730 (as the select circuit, column 7 lines 47-55 replacing the charge pump 530 & filter 540 FIG.5, column 7, lines 47-49) receiving the SLOWER signal and a FASTER signal (as the second control signal) to select the SLOWER or the FAST and to output the $TUNE_0$ - $TUNE_{N-1}$ signal (the selected control signal) to the continuously adjustable delay circuit 800 to adjust the phase of the clock (column 6 lines 44-50, wherein the circuit 300 in FIG.3 is the circuit 800 in FIG.7).

Regarding **claims 2 & 12**, in FIG.9A Kyles et al. teaches the flip-flops 910 & 920 (as the receive circuit) receiving the RECEIVE DATA clocked (sampled) into the flip-flops by the RECOVERED CLOCK (column 8 lines 46-54).

Regarding claims 3 & 13, in FIG.7, Kyles et al. teaches the adjustable delay circuit 800 outputting multiple clocks (CLOCKI, CLOCKZ, and RECOVERED CLOCKI; and the PHASE DETECT 500 comprising the flip-flops 910 & 920 (as the receive circuit) receiving the RECEIVE DATA clocked (sampled) into the flip-flops by the RECOVERED CLOCK (column 8 lines 46-60); and the gates 916 & 926 (the phase control circuit) outputs the FAST or SLOWER to indicate the lag or lead (column 8 line 65-column 9 line 2).

Regarding **claims 4-5 & 14-15**, Kyles et al. teaches the generated SLOW signal having two components/states being active or being not active (column 8 line 65-column 9 line 2) based on the RECOVERED CLOCK lagging or leading the RECEIVED DATA.

Regarding **claims 6 & 7**, in FIG.9A Kyles et al. teaches the first control signal is

an variable width pulse having a voltage/current level to indicate the phase difference (column 9 lines 3-10).

Regarding **claims 8 & 16**, in FIG.7, Kyles et al. teaches receiving the SELECT SIGNAL provided by the external device (the PATH SELECT 600).

Regarding **claims 9 & 17-18**, in FIG.6A & FIG.6B, Kyles et al. teaches the SELECT signal having a first and a second state based on the value stored in the flip-flop 620 which receives the ENABLE (command) to store the value, and in FIG.7 the MUX 516 (a circuitry) selecting the SLOWER signal or FASTER signal based on the states of the SELECT signal.

Regarding **claim 10**, in FIG.7, Kyles et al. teaches the multiplexer 516 & MUX 518) in the select circuit (the MUX 516, the MUX 518 and the shih register 730).

Regarding **claims 35-36**, in FIG.7, Kyles et al. teaches a system comprising a signal line receiving the RECEIVE DATA and a device 700 (the receive device) of receiving clocking signal and the RECEIVE DATA to recover the clock and the data, the device comprises a phase detect 520 (as the control circuit) receiving a RECEIVE DATA (as an input signal) to generate' a SLOWER (as the first control signal) based on the phase difference of the RECEIVE DATA and the RECOVERED CLOCK (column 6 lines 23-32); the MIJX 516, the MUX 518 and the shih register 730 (as the select circuit, column 7 lines 47-55) receiving the SLOWER signal and a FASTER signal (as the second control signal) to select the SLOWER or the FAST controlled by the SELECT signal based on the condition at $\Delta t = T$ (having a first mode value, in FIG.4 where the negative/positive TUNE is based on faster or slower of the chosen clock (clock1 or

clock2), column 6 lines 8-16) and to output the TUNE₀- TUNE_{N-1} signal to the continuously adjustable delay circuit 800 to adjust the phase of the clock (column 6 lines 44-50, wherein the circuit 300 in FIG.3 is the circuit 800 in FIG.7); and the PATH SELECT 600 (the control device) to provide the SELECT signal.

Regarding **claim 38**, in FIG.4, Kyles et al. teaches one mode value (positive tuning) at time interval T₀ to T₁, after this interval a second mode value (negative tuning) at time interval T₁ to T₂ that the SELECT signal responsive to.

Regarding **claims 40-43**, the limitation recites that the different part of the receiver can be implemented in different arrangements. The implementing in different arrangements does not affect the subject matter of the inventions cited in the apparatus claim 35 wherein a signal line, a receive device, and a control device are included, hence the limitation is a design choice.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 52-58 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cao et al. (US 6,725,408 B1) in view of Kyles et al. (US 6,008,680).

Regarding **claim 52**, in FIG.2, Cao et al. teaches a method and a device for implementing built-in self-test for multi-channel transceivers (column 1 lines 14-17,

column 3 lines 14-20). The device comprises a Test Pattern Generator (TPG 22) to generate a pseudo-random test pattern (as the first test signal, column 3 lines 37-39), a MUX 14 (as the receive circuit) to receive the PN test pattern based on the CLK; a CDR 10 (the clock data recovery circuit); and a TRE 24 (Test Result Evaluator as the compare circuit, column 3 lines 45-51) comparing the test pattern and the received from the DEMUX 12, however does not detail the CDR.

In FIG.7, Kyles et al. teaches a CDR circuit, the circuit comprises a phase detect 520 (as the control circuit) receiving a RECEIVE DATA (as an input signal) to generate a SLOWER (as the first control signal) based on the phase difference of the RECEIVE DATA and the RECOVERED CLOCK (column 6 lines 23-32 '680); the MUX 516, the MUX 518 and the shift register 730 (as the select circuit, column 7 lines 47-55 '680) receiving the LOWER signal and a FASTER signal (as the second control signal) to select the SLOWER or the FAST and to output the $TUNE_0$ - $TUNE_{N-1}$ signal to the continuously adjustable delay circuit 800 to adjust the phase of the clock (column 6 lines 44-50, wherein the circuit 300 in FIG.3 is the circuit 800 in FIG.7 '680).

At the time of the invention was made, it would have been obvious to one of ordinary skill in the art to implement the Cao et al.'s CDR by Kyles et al.'s teaching to receive the output signal from the MUX 14 as the RECEIVE DATA to have a continuously adjustable delay circuit for the purpose of being able adjust the changes in the phase of a signal without losing received data (column 3 lines 52-59 '408).

Regarding **claim 53**, in FIG.3, Cao et al. teaches the TPG is a linear feedback shift register to produce the PN test pattern (column 5 lines 34-38).

Regarding **claim 54**, in FIG.2, Cao et al. teaches the input selector 26 (as the transmit circuit as claimed) having the input 16 coupled to receive the test pattern switchably or the DATA (column 3 lines 22-27), and the output coupled to the MUX 14 switchably.

Regarding **claim 55**, in FIG.2, Cao et al. teaches the during the testing mode, the test pattern from the TPG fed to the MUX 14 (the receive circuit) via the input selector 26 being controlled by the mode (testing or operation, column 3 lines 22-27), hence the Cao et al.'s device provides a mode value/signal to the input selector 26 to select the test pattern or the data according to the mode value stored in a circuit of the device.

Regarding claims **56-57**, in FIG.4, Cao et al. teaches a signal generator in TRE to generate the signal generated from TPG by using the same signature provided to signature analyzer 40 (column 5 lines 2-7).

Regarding **claim 58**, in FIG.2, Cao et al. teaches the TPG 22 to provide the test pattern (the first test signal as the compare signal) to the TRE (column 4 lines 54-58).

Allowable Subject Matter

6. Claims 19-34, 45, 47-51 and 59 are allowed.
7. Claims 37 and 39 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
8. The following is a statement of reasons for the indication of allowable subject Matter:

The prior art of record fails to teach or suggest, alone or in a combination, among other things, at least a system of clock data recovery (CDR) circuits and its method as a whole, and the combination of elements and features, which includes a first CDR to recover clock and data signals from a first signal line and generate a first control signal, and a second CDR to recover clock and data signals from a second signal line and generate a second control signal wherein the first CDR adjust the phase of a first recovered clock in response to the first control signal, the second CDR comprising a select circuit to receive the first and second control signal to select one of the control signals responsive a select signal and adjusting the phase of a second recovered clock signal in response to the selected control signal, or selecting the control signals from a phase control port receiving control signals from external of a CDR instead of a phase control circuit in the CDR.

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

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the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Edith M. Chang whose telephone number is 571-272-3041. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay K. Patel can be reached on 571-272-2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Edith Chang
December 12, 2005


KHAI TRAN
PRIMARY EXAMINER